REMARKS

Claims 1-9, 11-13 and 18-21 are now present in this application.

Claims 1, 11-13, 18 and 19 have been amended, claims 10 and 14-17 have been canceled without prejudice or disclaimer of the subject matter contained therein and claims 20 and 21 have been presented. Reconsideration of the application, as amended, is respectfully requested.

Claims 1-7 and 10-19 stand rejected under 35 U.S.C.§ 103 as being unpatentable over Chiang et al. (US Patent No. 6,420,839) in view of Lin et al. (US Patent No. 6,856,519). Claims 8 and 9 stand rejected under 35 U.S.C.§ 103 as being unpatentable over Chiang et al. in view of Lin et al., and further in view of Fujimura et al. (US Patent No. 5,495,405). These rejections are respectfully traversed.

Claim 1, as amended, recites a combination of features that is neither disclosed nor suggested by the applied art. Specifically, Claim 1 recites that "a plurality of oscillation step-up circuits; and a digital control circuit, which has a digital switching signal generating circuit and a multiplex feedback-control calculating circuit, the digital switching signal generating circuit connects to each of the oscillation step-up circuits, generates sets of digital switching signals, and respectively transmits the sets of the digital switching signals to the oscillation step-up circuits, wherein the multiplex feedback-control calculating circuit has a control-calculating unit and an A/D converting unit, the control-calculating unit controls the digital switching signal generating circuit, and controls a phase and a duty cycle of each set of the digital switching signals generated by the digital switching signal generating circuit according to digital feedback signals from the A/D converting unit, the A/D converting unit converts feedback signals from the lights into the digital feedback signals, respectively, wherein a phase and a duty cycle of each set of the digital switching signals are controlled by the digital control circuit."

Both the digital switching signal generating circuit and the control-calculating unit of the digital control circuit are digital circuits. After converting the feedback signal from analog to

PAGE 10/14 * RCVD AT 11/16/2007 12:27:05 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/5 * DNIS:2738300 * CSID:7032058050 * DURATION (mm-ss):04-20

digital, the digital control circuit processes the digital feedback signal to generate the sets of digital switching signals in all digital without analog signal processing.

For further explanation, an example is provided below. For example, the control-calculating unit may include a memory, a counter and a comparator. The memory stores one or one more target values respective to each sets of the digital switching signals driving the oscillation step-up circuits. The counter counts a counting value. The comparator is electrically connected to the counter and the memory to generate triggering signals whenever the counting value matches the target counting value. The triggering signals trigger the digital switching signal generating circuit to generate the sets of the digital switching signals to the oscillation step-up circuits in sequence. The time interval between the sequential sets of the digital switching signals are controlled by the corresponding target value. Thus, the target values can be modified to change the time interval between the sequential lights turned on or off because lights are driven by the corresponding oscillation step-up circuits.

In this example, the digital switching signal generating circuit may include a register array and a logic array. The registers of the register array are triggered by the corresponding triggering signals and hold the value of the triggering signals. A digital pulse width modulation signal is inputted into the AND gates. Each value of the triggering signals are respectively inputted into the AND gates, such that the value of the triggering signal control the digital pulse width modulation signal to be the digital switching signals output from the respective AND gates. It should be noted that the memory, the counter, the comparator, the register array and the AND gates descript above are descript for explanation and are not for restricting implementation of the control-calculating unit and the digital switching signal generating circuit.

The Examiner admits that Chiang fails to disclose a digital control circuit. Applicant agrees. However, the Examiner alleges that Chiang discloses a plurality of oscillation step-up circuits. Applicant respectfully disagrees. As disclosed in the present application, an oscillation step-up circuit includes a switching unit and a resonance step-up unit, where the resonance step-

PAGE 11/14 * RCVD AT 11/16/2007 12:27:05 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/5 * DNIS:2738300 * CSID:7032058050 * DURATION (mm-ss):04-20

up unit may contain a transformer. Chiang, disclosing multiple transformers alone, does not necessarily disclose a plurality of oscillation step-up circuits.

The secondary reference to Lin is the same as Chiang in that it also fails to disclose a plurality of oscillation step-up circuits. Lin only discloses a single Royer circuit with transformer to drive two CCFL loads.

Furthermore, the Examiner relies upon Lin for disclosing a digital control circuit. Lin discloses an integrated circuit inverter controller, which generates switch drive signals. However, the integrated circuit inverter controller is not a digital control circuit.

First, a circuit generating switch drive signals alone is not necessarily a digital control circuit. The Lin reference discloses an analog circuit consisting of the comparator 42 and the CT signal 14 processes the feedback signal to generate signals controlling the switch logic driver. The CT signal 14 is an analog saw signal, and DC signal 52 generated based on the voltage and current feedback signal is input into the comparator 42.

The Lin reference discloses an ADC for converting the voltage feedback signal and a digital dimming circuit for generating a burst signal. However, the burst signal is applied to control the voltage level of the node. When the burst signal is not asserted, the voltage level of the node is controlled by the current feedback signal. It is therefore that the DC signal from the node behaves in an analog fashion, not digital.

The DC signal 52 controls the duty cycle of the signal generated by the comparator 42. The signal generated by comparator 42 represents the intersection between the lowest value of the CT signal 14 and the DC signal 52. It is well known in the PRIOR ART to generate a signal controlling its duty cycle by the analog CT signal 14, analog DC signal 52 and analog voltage comparator 42. The Lin reference does not processing the feedback signal in the control circuit all in digital after converting the feedback signal from analog to digital.

PAGE 12/14 * RCVD AT 11/16/2007 12:27:05 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/5 * DNIS:2738300 * CSID:7032058050 * DURATION (mm-ss):04-20

Second, Lin fails to disclose or teach, as in claim 1, "a digital control circuit, which has a digital switching signal generating circuit and a multiplex feedback-control calculating circuit, the digital switching signal generating circuit connects to each of the oscillation step-up circuits, generates sets of digital switching signals, and respectively transmits the sets of the digital switching signals to the oscillation step-up circuits, wherein the multiplex feedback-control calculating circuit has a control-calculating unit and an A/D converting unit, the control-calculating unit controls the digital switching signal generating circuit, and controls a phase and a duty cycle of each set of the digital switching signals generated by the digital switching signal generating circuit according to digital feedback signals from the A/D converting unit, the A/D converting unit converts feedback signals from the lights into the digital feedback signals, respectively, wherein a phase and a duty cycle of each set of the digital switching signals are controlled by the digital control circuit." As discussed above, Lin, fails to disclose a plurality of oscillation step-up circuits, and therefore fails to disclose a digital control circuit, which connects to each of the oscillation step-up circuits and generates sets of digital switching signals. Also, as pointed out by the Examiner in column 2, lines 60-61 of Lin, only pulse width, not both the phase and the duty cycle, of the switch driver signal is controlled.

Since both Chiang and Lin fail to disclose a plurality of oscillation step-up circuits and a digital control circuit, Applicant respectfully submits that claim 1 and its dependent claims clearly define over the teachings of Chiang and Lin. The secondary reference to Fujimura does not overcome these deficiencies. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. 103 are respectfully requested.

It is additionally noted that with respect to dependent claim 11, both Chiang and Lin fail to disclose that "the multiplex feedback-control calculating circuit is a digital single-chip microprocessor." The integrated circuit disclosed in Lin is not necessarily as the Examiner alleges a digital single-chip microprocessor.

With respect to dependent claim 12, both Chiang and Lin fail to disclose "an A/D converting unit, which electrically connects to the multiplex unit and converts the feedback signals into digital feedback signals, respectively; and a control-calculating unit, which controls

the multiplex unit and further controls the digital switching signal generating circuit according to the digital feedback signals." The A/D converting unit in Lin alleged by the Examiner does not convert the feedback signals into digital feedback signals. Also, there exists no control-calculating unit in Lin to further control the digital switching signal generating circuit according to the digital feedback signals.

In view of the above amendment, applicant believes the pending application is in condition for allowance. The 35 USC 103 rejections should be overcome and withdrawn and all claims should be in condition for allowance. An early Notice of Allowance is earnestly solicited.

Conclusion

Because the additional prior art cited by the Examiner has been included merely to show the state of prior art and is not being utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

By _____
Joe McKinney Muncy
Registration No.: 32,334
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East, P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

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PAGE 14/14 * RCVD AT 11/16/2007 12:27:05 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/5 * DNIS:2738300 * CSID:7032058050 * DURATION (mm-ss):04-20